B6 Cont'd

the seventh step of forming a dielectric film so as to cover a surface of said first conductive film; and

the eighth step of forming a second conductive film so as to cover said dielectric film opposing said first conductive film through said dielectric film.

REMARKS

Claims 28-45 are pending in the application. Favorable reconsideration of the case is requested.

Withdrawal of the objection to Figs. 1A and 10A is requested in light of the drawing correction enclosed herein.

Withdrawal of the objection to the specification is requested. The requested changes to the specification have been made to improve its clarity. A new title has been entered in the case which is more descriptive of the disclosed subject matter.

Withdrawal of the objection to claim 32 is requested in light of the amendments made herein.

Withdrawal of the rejection of the claims under 35 U.S.C. § 112 is requested in light of the amendments made herein.

Withdrawal of the rejection of claims 32-34, 36, and 42-43, under 35 U.S.C. § 102(e) as being anticipated by Schoenfeld et al., is requested. The present invention, as exemplified by amended claim 32, is directed to a method for fabricating a semiconductor. The method employs a process for forming an insulated gate structure on a semiconductor. In carrying out the invention, a mask pattern is formed over a insulating film and gate electrode in an element active region. The mask pattern includes first and second openings. The first opening is etched so that the opening extends to an element isolation structure formed in the substrate. The second opening forms a recess having a conductive film along the bottom thereof.

In reviewing the Schoenfeld et al. reference, it is not evident where there is any structure corresponding to the first opening, which is connected to an element isolation

structure. Schoenfeld et al. illustrates the formation of nodes 132 which are storage devices. The nodes are formed by a masking step illustrated in Fig. 2, which, following etching, produces nodes such as shown in Fig. 3. The nodes do not include any structure which could be considered a first opening extending to the element isolation structure. Accordingly, the rejected claims can not be anticipated or suggested by Schoenfeld et al. which fails to disclose this structure.

Withdrawal of the rejection of claims 36-38 and 40 under 35 U.S.C. § 102(e) as being anticipated by Tseng is requested. The patent to Tseng illustrates the formation of a node electrode for a DRAM. The node electrode is illustrated with respect to Figs. 5 and 6 as being formed from an opening 13c which includes a photoresist material 15. The photoresist 15 masks the structure so that a polysilicon column 11b can be formed as shown in Fig. 7. The column is thereafter covered with a plate electrode 17.

The steps illustrated do not disclose any masking step which would provide two openings, one of which extends down to an element isolation structure. Accordingly, it is not seen how the reference can anticipate or render obvious the subject matter of the rejected claims, all of which include such structure.

Withdrawal of the rejection of claims 36-39 and 41, as being anticipated under 35 U.S.C. § 102(b) by Iwamatsu et al. is requested. The Iwamatsu et al. reference illustrates a method for making a semiconductor device. In reviewing the reference, however, there is no disclosure of any masking step which provides first and second openings, the first of which is etched so that it reaches an element isolation structure along the substrate. The characterization in item 3 of the Office Action, that Fig. 7 shows a mask pattern 21 having two openings (one on each side of the mask shown in Fig. 7), is believed to be in error. In reviewing Fig. 7, it is not seen where item 21 constitutes a mask having first and second openings, so that etching may be effected down to an element isolation structure in one opening. Item 21 does not appear to have any openings, or holes, and no holes formed down to an element isolation structure.

Withdrawal of the rejection of claims 35 and 44, under 35 U.S.C. § 103(a) as being unpatentable over Schoenfeld et al. in view of Tseng is requested. As was noted with respect to the previous rejections, neither Schoenfeld et al. nor Tseng disclose or suggest a mask step wherein photoresist is provided having two openings, one of which permits removal of conductor and insulation down to the element isolation structure, and the other of which extends to a lesser depth, having a metal layer along the bottom thereof. Accordingly, since neither reference shows or discloses this structure, any combination thereof cannot yield or suggest the subject matter of the present claims.

Withdrawal of the rejection of claim 45 under 35 U.S.C. § 103(a) as being unpatentable over Schoenfeld et al. in view of Eaton, Jr. et al. is requested. Claim 45 is dependent from claim 42, and carries all the limitations thereof. Accordingly, withdrawal of the rejection is believed to be in order.

In view of the foregoing, favorable reconsideration is requested.

In the event the Examiner believes an interview might serve to advance the prosecution of this application in any way, the undersigned attorney is available at the telephone number noted below.

The Director is hereby authorized to charge any fees, or credit any overpayment, associated with this communication, including any extension fees, to Deposit Account No. 22-0185.

Respectfully submitted,

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present invention is a semiconductor device including an element active region defined by forming an element isolation structure on a semiconductor substrate, comprising an insulating film formed on the semiconductor substrate in the element active region, and a charge storage film patterned on the insulating film, wherein the charge storage film is formed across the element isolation structure and has a hole on the element isolation structure, and at least a portion of a bottom surface of the hole reaches a surface layer of the element isolation structure.

Still another aspect of the semiconductor device of the present invention is a semiconductor device including a plurality of element isolation regions defined by forming an element isolation structure on a semiconductor substrate, comprising an island-like charge storage film formed across the element isolation structure and the element active regions and having a recess, a dielectric film so formed as to cover a surface of the charge storage film, and a conductive film formed on the dielectric film and capacitively coupled with the charge storage film, wherein the charge storage film is formed in each of the element active regions, and an upper surface of each of the charge storage films is planarized by CMP and flush with an upper surface of an adjacent charge storage film.

A method of fabricating a semiconductor device according to the present invention comprises the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate, the second step of forming an insulating film on the semiconductor substrate in the element active region, the

third step of forming a first conductive film on an entire surface of the semiconductor substrate including the insulating film and the element isolation structure, the fourth step of forming a mask pattern having first and second openings on the first conductive film, the fifth step of etching the first conductive film until the element isolation structure is exposed in the first opening by using the mask pattern as a mask, thereby dividing the first conductive film, and simultaneously forming a recess in the second opening by leaving the first conductive film behind on a bottom of the reverse, the sixth step of forming a dielectric film so as to cover a surface of the first conductive film, and the seventh step of forming a second conductive film on the dielectric film and opposing the second conductive film to the first conductive film through the dielectric film. 14

Another aspect of the method of fabricating a semiconductor device according to the present invention comprises the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate, the second step of forming a gate insulating film and a gate electrode in the element active region, the third step of doping an impurity into the second substrate to form a pair of impurity diffusion layers in surface regions of the semiconductor substrate on two sides of the gate electrode, the fourth step of forming a first conductive film electrically connected to one of the impurity diffusion layers, the fifth step of forming a mask pattern having at least first and second openings on the first conductive film, the sixth step of etching the first conductive film by using the mask pattern as a mask,

thereby dividing the first conductive film in the first opening, and simultaneously forming a recess in the second opening by leaving the first conductive film behind on a bottom of the recess of the seventh step of forming a dielectric film so as to cover a surface of the first conductive film, and the eighth step of forming a second conductive film on the dielectric film and opposing the second conductive film to the first conductive film through the dielectric film.

Still another aspect of the method of fabricating a semiconductor device according to the present invention comprises the first step of forming a first conductive film in an insulating film region on a semiconductor substrate, the second step of forming a mask pattern having two types of openings on the first conductive film, the third step of etching the first conductive film by using the mask pattern as a mask, thereby dividing the first conductive film conforming to a shape of one of the openings, and simultaneously forming at least one recess in a surface of the divided first conductive film conforming to a shape of the other opening, the fourth step of forming an insulating film so as to cover a surface of the first conductive film, and the fifth step of forming a second conductive film so as to cover a surface of the insulating film and opposing the second conductive film to the first conductive film through the insulating film.

Still another aspect of the method of fabricating a semiconductor device according to the present invention comprises the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate, the second step of forming an

insulating film on the semiconductor substrate in the element active region, the third step of forming a first conductive film on an entire surface including the insulating film and the element isolation structure, the fourth step of forming a mask pattern having at least first and second openings on the first conductive film, the fifth step of etching the first conductive film until the element isolation structure is exposed in the first and second openings by using the mask pattern as a mask, thereby dividing the first conductive film below the first opening, and simultaneously forming a hole extending through the first conductive film below the second opening, the sixth step of forming a dielectric film so as to cover the first conductive film, and the seventh step of forming a second conductive film on the dielectric film and opposing the second conductive film to the first conductive film through the dielectric film.

Still another aspect of the method of fabricating a semiconductor device according to the present invention comprises the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate, the second step of forming a gate oxide film and a gate electrode on the semiconductor substrate in the element active region, the third step of doping an impurity into the semiconductor substrate in the element active region to form a pair of impurity diffusion layers in surface regions of the semiconductor substrate on two sides of the gate electrode, the fourth step of forming a first conductive film electrically connected to one of the impurity diffusion layers, the fifth step of forming a mask